REMARKS

I. Introduction

Claims 2-8, 11, and 12 are pending in this application, of which claims 2 and 12 are independent. Claim 11 was previously withdrawn from consideration. In this Amendment, claims 2 and 12 have been amended. Support can be found in, for example, Fig. 2 and relevant description of the specification. Care has been exercised not to introduce new matter.

A Request for Continued Examination is concurrently filed with this Amendment.

II. Rejections of Claims Under 35 U.S.C. § 112, second paragraph

Claims 2-8 were rejected under 35 U.S.C. § 112, second paragraph, because there was a lack of antecedent basis for the limitation "the transferred-word storing means." Applicant respectfully submits that the limitation in claim 2, as amended herein, has a proper antecedent basis. Hence, claim 2 is definite as presented above. Withdrawal of this rejection is respectfully requested.

III. Rejections of Independent Claims Under 35 U.S.C. § 103

Claims 2 and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Admitted Prior Art (hereinafter "AAPA") in view of Kato (U.S. Patent No. 5,333,290, hereinafter "Kato").

Applicant submits that the AAPA and Kato, either individually or in combination, do not disclose or suggest a data transfer control system including all the limitations recited in independent claim 2. Specifically, the applied combination does not teach, among other things, the following limitations as recited in claim 2:

> bus cycle controlling means for controlling the data transfer such that, during a burst transfer, in a single bus cycle, during the single bus cycle, the bus is driven continuously and a write control line of the bus is placed in a write-enabled state

> for a one-word data transfer period and is placed in a write-disabled state for an (N-1) words data transfer period and the operation is repeated for M(2<M) times periodically, the M being the number of words of data which are to be transferred and stored in the transferred-word number storing means, ...

In response to the January 18, 2008 reply, the Examiner asserted as follows (see paragraph 2 of the Office Action) (emphasis in original):

> AAPA teaches M being the number of words of data which are to be transferred and stored in the transferred-word number means, wherein M>1 as there are at least Data 1 and Data 2 to be transferred (Drawings, transferred-word number register 103 of Fig. 19 and Specification, page 1, l. 9 to page 2, l. 7).

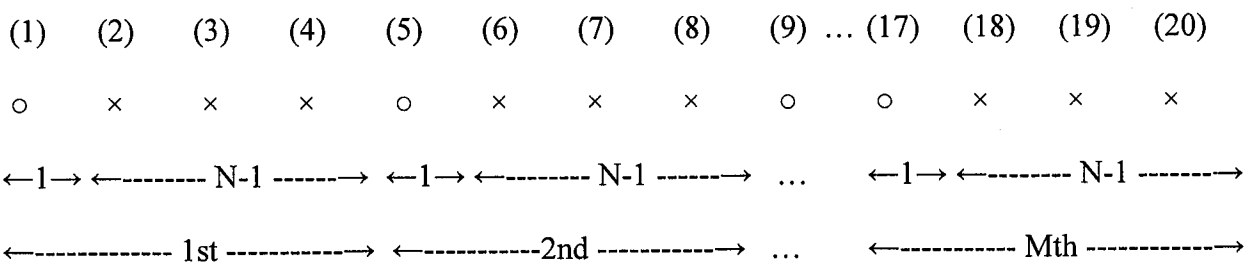
Applicant submits that the Examiner overlooked the claimed limitations. Claim 2 recites, "during the single bus cycle, the bus is driven continuously and a write control line of the bus is placed in a write-enabled state for a one-word data transfer period and is placed in a write-disabled state for an (N-1) words data transfer period and the operation is repeated for M(2<M) times periodically" (emphasis added). The AAPA describes, "the bus cycle is caused twice to perform a single transfer operation twice, whereby the two pieces of data are transferred to two separate addresses" (page 2, lines 6-7 of the specification). The AAPA does not teach transferring Data 1 and Data 2 in a single bus cycle, but teaches transferring Data 1 and Data 2 in respective single bus cycles.

The Examiner further asserted as follows (paragraph 2 of the Office Action) (second emphasis added):

> Kato teaches the operation (e.g. operation for data transferring) is repeated for M(1<M) times (Fig. 1, col. 1, ll. 47-67 and col. 3, l. 43 to col. 4, l. 25) as during a single burst of data transfer, when memory areas exist that is not to be read/write, those areas will be bypassed (jumped); therefore, when there is at least one bypass area in the single burst data transferring, M would be greater than 1.

Applicant submits that the Examiner still misunderstood Kato and the claimed subject matter. Applicant reiterates the explanation made in the previous response.

The claimed subject matter will be explained in accordance with the following figure where it is assumed that N is 4 (N is the number stored in the transfer interval storing means), and M is 5 (M is the number of words of data to be transferred and stored in the transferred-word number storing means). During (1) to (20) time frame, the operation is repeated five times to transfer five pieces of data to destination addresses, respectively, in a single bus cycle.



(1) to (20): time frame

○: write-enable

×: write-disable

According to Kato, it is possible to write DMA transferred data by bypassing JUMP START ADDRESS (16) and JUMP END ADDRESS (18). This corresponds to a situation where M=1 in claim 2. In other words, Kato addresses what happens only in, for example, time frame (1) to (4) in the above figure, where data is transferred at period (1), but not transferred at periods (2) to (4). However, Kato does not teach repeating the writing sequence for plural times during a single bus cycle. Kato simply discloses a resistor that designates a starting point and an end point for bypassing but it has no mechanism for designating how many times the bypassing is repeated. Therefore, Kato has to have L resistors (L is the number of repeating bypassing) in advance in order to achieve a repeat bypassing process, as claimed.

In contrast, the claimed system determines how many times bypassing is repeated according to the number M(2<M), the number M being stored in the transferred-word number storing means. The system can designate how many times bypassing is repeated with simple hardware. The AAPA and Kato is silent on, at a minimum, the number M(2<M). Again, the AAPA does not teach transferring Data 1 and Data 2 in a single bus cycle, and Kato does not teach any mechanism for designating how many times the bypassing is repeated.

Based on the foregoing, the AAPA and Kato, either individually or in combination, do not disclose or suggest a data transfer control system including all the limitations recited in independent claim 2. The above discussion is applicable to independent claim 12. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claims and favorable consideration thereof.

III. Rejection of Dependent Claims Under 35 U.S.C. § 103

Claims 3 and 7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Kato, and further in view of Sheafor et al. and Kreifels; claim 4 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Kato, and further in view of Fabre; claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA, Kato, Sheafor et al., and Kreifels, and further in view of Fabre; claim 6 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA and Kato, and further in view of Kreifels; and claim 8 has been rejected under 35 U.S.C. §103(a) as being unpatentable over the AAPA, Kato, and Fabre, and further in view of Kreifels.

Claims 3-8 depend from independent claim 1. Applicant incorporates herein the arguments made in response to the rejection of independent claim 1 under 35 U.S.C. §103 for

obviousness predicated upon the AAPA and Kato. The Examiner's additional comments and reference to Sheafor et al., Kreifels, and Fabre do not cure the previously argued deficiencies of the applied combination of the AAPA and Kato.

Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 3-8 and favorable consideration thereof.

IV. Conclusion

In view of the above amendments and remarks, Applicants submit that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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